



JSPM's  
**Bhivarabai Sawant Institute of Technology and Research,  
Wagholi, Pune.**  
(Approved by AICTE, Delhi & Govt. of Maharashtra, affiliated to Savitribai Phule Pune University)  
Gat. No.720, Pune-Nagar Road, Wagholi, Pune-412207



## CYNOSURE 2K19

### **Name of Event: *Quick Circuit Making***

- Objective:**
1. To express their talent in the field of electronic circuit designing.
  2. To analyze and design simple electronic circuits.
- Staff Co-coordinator:**
1. Prof. Sheetal S. Dubal (BSIOTR)
  2. Prof. Rahul K.Sarawale (ICOER)
- Student Co-coordinator:**
1. Ms. Snehal Satav (BSIOTR)
  2. Ms. Gayatri Bhavsar (ICOER)
- Venue:** B4 Building, JSPM Wagholi Campus Room no:306 & 407
- Date:** 17/01/2019
- Registration Fee:** Rs. 100/- per group (Maximum Two Participants per group)
- Prizes :**
- 1<sup>st</sup> Rs. 1000/-
- 2<sup>nd</sup> Rs. 750/-
- Winner:**
- 1<sup>st</sup> Mr. Ashwin Abhang(BSIOTR,Wagholi)
- 2<sup>nd</sup> Shreyas Pawar (ICOER,Wagholi)  
Asad Shaikh (ICOER,Wagholi)
- Number of Entries:** 25

## **Rules and Regulation of the Event:**

### **Round I: Multiple Choice Questions**

1. 25 Number of objective questions are to be solved within 30 min.
2. Objective questions will be based on subjects like Basic Electronics, Basic Electrical, Electronic Devices and Circuits (EDC), Digital Logic Design (DLD), Linear Integrated Circuits (LIC).
3. Use of Scientific Calculator is allowed.
4. Make a Tick Mark ( $\checkmark$ ) on appropriate choice.
5. Once tick mark is done on the choice it cannot be altered. For multiple tick marks, zero marks will be given.
6. If book or any other supporting material is found, that group will be disqualified from the competition.
7. Result of Round-I will be displayed on Notice Board.
8. After evaluation selected groups will appear for second round.

### **Round II: Circuit design and implementation**

1. Problem statements will be given for circuit design and implementation to each group or team.
2. On completion, the final circuit has to work for all the test cases.
3. On completion of first circuit implementation, Group may implement another circuit within prescribed time (30minutes). Number of circuits implemented will also be the criteria for selection.
4. It will also be judged on the basis of circuit simplicity, efficiency, and ability to fulfill criterion given in the problem statement.
5. In case of a tie, judging will be done on the methodology followed to achieve the solution to the problems. The decision of the judges will be final and binding.
6. In case of incomplete solution, it shall be judged on the method of approach and closeness to the real solution.
7. The verdict of the respected Judge shall be final and binding.

**Inauguration of an event by Dr. Pratapsinh K. Desai (President ISTE, New Delhi) and Dr. Dayanand Tiwari:**



**Glimpses of an event:**



**Inspection by Judge:**



**Prize Distribution to winners:**



Prof. T.V.Kafare  
ETSA Coordinator

Dr. Y.S. Angal  
HOD E&TC  
H. O. D.

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